DIGITAL DESIGN

Naval Undersea Warfare Center, Division Newport

AFTER OPTIMIZATION
(Parallel Operations)

| 2,660 ns | 2,680 ns | 2,700 ns | 2,720 ns | 2,740 ns | 2,760 ns | 2,780 ns |

STEP **1** + STEP **1**   STEP **2** + STEP **2** ●●   STEP **3** + STEP **3**

RESULT **1**   RESULT **2** ●●   RESULT **N**

FINAL RESULT

BEFORE OPTIMIZATION
(Sequential)

STEP **1**   STEP **1**
+
STEP **2**   STEP **2**
+
⋮   ⋮
STEP **N**   STEP **N**
+
RESULT

FINAL RESULT
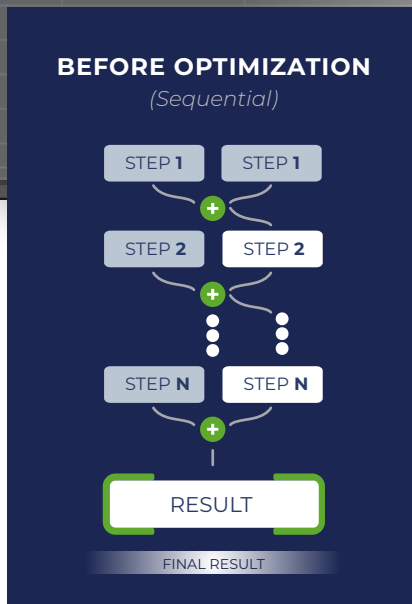
An ongoing issue in computer hardware design is the design of floating point hardware which is both standard compliant (IEEE-754) and efficient in both size and speed while delivering the correct precision in results.

These digital design prototypes were tested against the present Xilinx and Altera floating-point FGPA designs and performed **30%-50%** better in size and/or speed as compared to commercial IEEE-754 hardware.

Potential Commercial Uses

- Design applies to any floating point hardware
- Implementation into standard floating point units
- Results scale up with hardware and fabrication design improvements

INITIAL PROTOTYPE AVAILABLE

PATENT NUMBER(S): 14/535384, 17/575703, and 17/123194

NAVSEA WARFARE CENTERS NEWPORT

Partnering interest? Contact: Technology Partnership Office
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TPO
TECHNOLOGY PARTNERSHIP OFFICE